Design and Simulation of Low Voltage Operational Amplifier

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Abstract—This report describes the design and simulation of a CMOS low voltage operational amplifier with input common-mode range extending above \( V_{DD} \) and below ground and can drive relatively large load capacitors. The amplifier uses a differential amplifier and push-pull amplifier configuration. Furthermore, the circuit is fully functional with a \( V_{DD} \) as low as 2V. Design considerations provide a NMOS size of \( 120/2 \) and PMOS size of \( 400/2 \) (with \( 0.6 \mu \) scale factor) and bias current of \( 5 \mu A \).

Keywords—Low Voltage, Operational Amplifier, Push-Pull, Differential Amplifier, Beta-Multiplier, Bias Current

I. INTRODUCTION

Low Voltage Operational Amplifiers (Op-Amp) are a necessity when designing electronics which operate on limited supply such as mobile phones are other low power electronics. Many modern designs are made with rail-to-rail output swing as well as input range. This documents the design process of a low voltage op-amp for fabrication in the C5 500nm process.

II. COMPONENT DESIGN

The main components of the low-voltage op-amp are the beta-multiplier and biasing circuit, differential amplifier, and push-pull amplifier.

To build these components, characterizing the devices for the beta-multiplier circuit and biasing circuit is essential. Understanding that the amplifier must operate with a minimum \( V_{DD} \) of 2V indicates that the devices must be designed to operate with a minimum overdrive voltage. A low overdrive voltage (relative to power supply) is obtainable by sizing your devices to operate with minimal \( V_{DS} \) or \( V_{SD} \) values, biasing the devices with a low bias current and placing the PMOS devices in their own well (tying the body to the source) to reduce the potential from the body of the NMOS.

Sweeping the \( V_{GS} \) of the device (NMOS) from 0 to 1V and holding the \( V_{DS} \) at constant 2V while plotting the derivative of the current flowing in the drain returns a graph which can obtain a good estimate of the Threshold voltage of the device. With an NMOS sized at \( 72 \mu/1.2 \mu \) the threshold \( (V_{THN}) \) would hold around 0.72V. Sweeping the \( V_{SG} \) while holding \( V_{SD} \) at 2V of a PMOS sized at \( 240 \mu/1.2 \mu \) returns a threshold of \( (V_{THP}) 0.9V \).
Selecting a low bias current can decrease the overdrive voltage of PMOS and NMOS devices (less pressure at the node to supply current) and for these devices. For the devices holding \( V_{GS} \) and sweeping \( V_{DS} \) from 0 to 200mV returned an IV curve indicating a 5\( \mu \)A bias current at a \( V_{DS} \) of 164mV and equivalent \( r_n \) around 400k\( \Omega \). Sweeping the \( V_{SD} \) while holding \( V_{SG} \) of the PMOS indicates 5\( \mu \)A bias current with \( V_{SD} \) of 411mV and equivalent \( r_n \) around 1.2M\( \Omega \).

Using these simulations as a base can help speed up the process of designing the Beta-Multiplier Reference circuit and subsequently the biasing circuit supplying voltages to the rest of the op-amp. Some further parameters identified and used to design the op-amp are listed in the following table.

![NMOS Characteristic Schematic & Curve II](image)

### Table 1: NMOS and PMOS Parameters
(Values shown are based off Bias Circuit SPICE Error Log)

<table>
<thead>
<tr>
<th>Parameter Type</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON Process Bias Current ( I_D )</td>
<td>5( \mu )A</td>
<td>5( \mu )A</td>
</tr>
<tr>
<td>( W/L )</td>
<td>120/2</td>
<td>400/2</td>
</tr>
<tr>
<td>( V_{GS} ) and ( V_{SG} )</td>
<td>0.72 V</td>
<td>0.92 V</td>
</tr>
<tr>
<td>( V_{THN} ) and ( V_{THP} )</td>
<td>0.67 V</td>
<td>0.91 V</td>
</tr>
<tr>
<td>( dV_{THN,P}/dT )</td>
<td>0.6 mV/( ^\circ )C</td>
<td>0.6 mV/( ^\circ )C</td>
</tr>
<tr>
<td>( C'_{ox} )</td>
<td>2.5 fF/(( \mu m )^2)</td>
<td>2.5 fF/(( \mu m )^2)</td>
</tr>
<tr>
<td>( C_{oxn} ) and ( C_{exp} )</td>
<td>21.5 fF</td>
<td>104 fF</td>
</tr>
<tr>
<td>( C_{gsn} ) and ( C_{dgp} )</td>
<td>14.3 fF</td>
<td>69.4 fF</td>
</tr>
<tr>
<td>( g_{mn} ) and ( g_{mp} )</td>
<td>116 uA/V</td>
<td>111 uA/V</td>
</tr>
<tr>
<td>( r_{on} ) and ( r_{op} )</td>
<td>404K ( \Omega )</td>
<td>1.2M ( \Omega )</td>
</tr>
<tr>
<td>( g_{mn} r_{on} ) and ( g_{mp} r_{op} )</td>
<td>47.2 V/V</td>
<td>133.2 V/V</td>
</tr>
<tr>
<td>( \lambda_n ) and ( \lambda_p )</td>
<td>0.49 V(^{-1})</td>
<td>0.17 V(^{-1})</td>
</tr>
<tr>
<td>( f_{Tn} ) and ( f_{Tp} )</td>
<td>1.29 GHz</td>
<td>255 MHz</td>
</tr>
</tbody>
</table>

### ON C5 Process
(Values based on 2V \( V_{DD} \) and 5\( \mu \)A bias current)

### Beta-Multiplier Reference

The first component designed in the device is the Beta-Multiplier Reference (BMR) circuit. This circuit supplies a constant bias voltage and current used to build the full biasing circuit. The BMR is built based on the bias currents and voltages given in Table 1 and is a self-biasing MOSFET only reference circuit. A start-up circuit is built into the design of the BMR to prevent the self-biased circuit from closing up and having zero current flowing in the circuit. However, the start-up
circuit should have no effect on the operation of the BMR circuit other than preventing it from operating in an “off” configuration. When designing the start-up circuit it is important to consider the sizing of the MSU3 device because it can leak current into the BMR. As $V_{DD}$ increases this can cause the reference current to increase as well if not properly sized. Since the C5 process is a short-channel process, and is built to operate under a reliably low $V_{DD}$, the BMR can be susceptible to variations in $V_{DD}$. To prevent the supply from having such an effect on the circuit that provides a steady bias current and voltage, a differential amplifier is added to the design to regulate and reduce variation of the drain-to-source voltages of the NMOS in the BMR. With this regulation however, it can cause instability and force currents to oscillate not only in the BMR, but further down the line in the device. To compensate for this instability, MOSCAPs are placed on the output of our produced bias voltages to provide a significant load that may not be compensated for by the rest of the design.

\[ V_{SG} = V_{DD} - (V_{THP} + V_{SD,Sat}) \]

Using this Beta-Multiplier design, a full bias circuit can be built to provide references for the rest of the operational amplifier.

**B. Bias Circuit**

The bias circuit is designed to provide the various reference voltages required for the differential amplifier and push-pull amplifier components of the op-amp. Six bias voltages are used in the op-amp design which are established in the bias circuit. To provide a steady current in the rest of the device, a cascode structure is used to supply multiple PMOS and NMOS bias voltages. In a low-voltage design a wide-swing cascode design is required in order to keep all of the devices in saturation as it cannot supply enough voltage when there are $2 \times V_{GS}$ lost across the cascode structure alone. When the drop is decreased to $2 \times V_{DS,Sat} + V_{THN}$ the cascode structure can operate as expected. To generate a cascode voltage a folded cascode structure is used, which is biased with the voltages generated from the wide-swing cascode bias. However when operating with a $V_{DD}$ of 2V, there is a sacrifice made which is removing a cascoded device when generating NMOS and PMOS cascode voltages, which trades-off with current consistency in the rest of the circuit.

The BMR circuit is able to hold a steady 5µA current source when the VDD is varying from 1.5 to 5V as shown in Figure 3. The simulation also shows that the Vbiasn voltage holds steady while
As $V_{DD}$ varies (swept from 1.5 to 5V), the bias current that flows in the branches of $V_{BIAS1-4}$ is held constant at 5μA. The currents flowing in the $V_{CASN,P}$ branches increase linearly with $V_{DD}$ which is not ideal but this is caused by the lack of an additional cascode device in these branches holding the drain-source voltage fixed, which keeps the current constant. Without a higher potential, the current source will vary relative to changes in VDD.

C. Differential Amplifier

The differential amplifier (diff-amp) of the design is biased with $V_{BIAS1-4}$ voltages from the biasing circuit branches and is composed of equivalently sized NMOS and PMOS used in the biasing circuit. The diff-amp in used in this design is actually a PMOS diff-amp and NMOS diff-amp in parallel. The reason for this topology is meant to extend the input common-mode voltage beyond the rails, meaning above $V_{DD}$ and below ground. The diff-amp works in sync with a push-pull amplifier which is used to control and improve the output swing of the diff-amp. The push-pull amplifier compensates the extra current supplied by the NMOS and PMOS diff-amps by adding additional NMOS and PMOS current sources and sinks. The diff-amps were designed with split-length diff-pairing to create a low impedance node to feed back the $C_C$. Feeding back the capacitance back into this node improved the CMRR, PSRR and reduced the size of the required $C_C$ to meet an appropriate gain bandwidth product.

The current flowing through the branches mirrors the biasing circuit current of 5μA and the split-length diff-pairs work in series to provide the equivalent current. The transconductance of the diff-amp goes up when both NMOS and PMOS diff-amps are on e.g. changing the unity gain frequency of the op-amp relative to the following relationship:

$$f_{un} = \frac{g_{mns}+g_{mp}}{2\pi C_C}$$

When only one of the diff-amp is on the unity gain frequency is represented by:

$$f_{un} = \frac{g_{mns}}{2\pi C_C}$$

This relationship can cause distortion with variations in $V_{CM}$ because this causes the gain to vary relative to these changes.

D. Push-Pull Amplifier

The differential amplifier (diff-amp) of the design is biased with $V_{BIAS1-4}$ voltages from the biasing circuit branches and $V_{CASN,P}$ to bias the floating current sources in the common-source amplifier formed by the folded cascoded NMOS and PMOS structures, and this current is mirrored in the output buffer. Using an inverter-style topology as an output buffer allows the output to swing very close to $V_{DD}$ and ground. The operation of the push-pull
amplifier comes into play when the input current is positive and injected into the floating current source which will cause the node that the output PMOS gate is connected to rise, turning off the PMOS and further turning on the output buffer NMOS, while the inverse happens when the input current is negative (thus the name of the topology, push-pull).

The operational amplifier was then given a standard op-amp symbol for simulation and testing of the device.

An occasional issue with this design is that the gain can suffer when using a large load such as 1k which can reduce the gain significantly. Compensating for a large load can be done by sizing the output devices larger to provide significant current to supply a large load, however this increases the quiescent current of the circuit, which can increase the power consumption to an unusable point.

III. LOW VOLTAGE OPERATIONAL AMPLIFIER

The complete Operational amplifier design is shown below:
IV. simulations

This section shows operation of the low-voltage operational amplifier, as well as showing the limitations and trade-offs made when designing the amplifier.

A. DC Open-Loop Gain

![DC Open-Loop Gain Schematic & Simulation](image)

This slew rate can be cleaned up and have a higher slew-rate (closer to 2 or 3V/μs) however this would require lowering the value of our compensation capacitor which would send the gain bandwidth product much too high and the circuit would be power hungry, while also reducing the CMRR below specifications, although it would be close.

B. Slew-Rate

![Slew-Rate Schematic & Simulation](image)

C. Step Response

![Step Response Schematic & Simulation](image)
D. Common-Mode Rejection Ratio (CMRR)

![CMRR Schematic & Simulation](image1)

Fig 12: CMRR Schematic & Simulation

The PSRR of the operational amplifier could not meet the intended value of 90-dB at 100kHz. The PSRR specification was sacrificed in order to obtain a CMRR that met the specification of 90-dB at 100kHz. The argument could be made that this is most acceptable specification to not be met, because there is a possibility for a power supply filter or something similar to filter out the noise and prevent it from translating into our output (either from ground or VDD). CMRR cannot be adjusted after chip fabrication, but there are still adjustments that can be made externally to improve PSRR of the operational amplifier.

E. Power Supply Rejection Ratio (PSRR)

![Power Supply Rejection Ratio Schematic & Simulation](image2)

Fig 13: PSRR Schematic & Simulation

![Output Swing Schematic & Simulation](image3)

Fig 14: Output Swing Schematic & Simulation

F. Output Swing

The PSRR of the operational amplifier could not meet the intended value of 90-dB at 100kHz. The PSRR specification was sacrificed in order to obtain a CMRR that met the specification of 90-dB at 100kHz. The argument could be made that this is most acceptable specification to not be met, because there is a possibility for a power supply filter or something similar to filter out the noise and prevent it from translating into our output (either from ground or VDD). CMRR cannot be adjusted after chip fabrication, but there are still adjustments that can be made externally to improve PSRR of the operational amplifier.
G. Input CMR as a function of $V_{DD}$

![Graph showing CMR as a function of $V_{DD}$](image)

**Low-Voltage Op-Amp Parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Open-Loop Gain</td>
<td>110 dB</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>6.17 MHz</td>
</tr>
<tr>
<td>3-dB Frequency</td>
<td>$f_{3\text{dB}} = 13.5$ Hz</td>
</tr>
<tr>
<td>Slew-Rate</td>
<td>1.3 V/μs</td>
</tr>
<tr>
<td>CMRR at 100 kHz</td>
<td>94 dB</td>
</tr>
<tr>
<td>PSRR at 100 kHz</td>
<td>56 dB</td>
</tr>
</tbody>
</table>
| Input Common Mode Range | $\text{CMR}_{\text{MAX}} = V_{DD} + 1$ V  
|                         | $\text{CMR}_{\text{MIN}} = 0$ - 1 V |
| Output Swing            | 5 mV to 1.99 V               |
| Power Consumption       | $P_{IN} = 337μA \times 2$ V  
|                         | $P_{IN} = 674μW$             |
| VDD Operating Range     | $V_{DD} = 2$ V to 5 V        |

Table 2: Summary of Results

A common use of the device is Inverting Op Amp Topology which controls the gain using external resistors.

![Inverting Op-Amp Schematic & Simulation](image)

With the current configuration, of a feedback resistor of 100k and an input resistor 1k, we should receive a gain $A_v = 100$. Even with minimum resistive load and maximum capacitive load, the op-amp is able to produce the expected gain and the output will swing within 100 mV of VDD and Ground.

V. Conclusion

The low-voltage op-amp provided in this design meets previously set out expectations with exception to the PSRR. Overall the design is acceptable but there are still some parameters to consider when designing the device such as what the device’s main application will be, which can influence which parameters you would chose to meet.